A PWM CONTROL CIRCUIT FOR THE POST-ADJUSTMENT OF MULTI-OUTPUT SWITCHING POWER SUPPLIES

Field of the Invention

The present invention relates to power supplies, and, more particularly, to switching power supplies having a plurality of outputs each provided with a respective pulse-width modulation (PWM) regulator and control circuits therefor.

Background of the Invention

Many electronic devices require two or more isolated, stable and precisely regulated supply voltages. For example, microprocessors require a precise supply voltage of 3.3V or less, together with a conventional supply voltage of 5V. As these devices reach ever-smaller dimensions, they require increasingly higher power and higher operating efficiency. The trend of reducing component dimensions, combined with the trend of providing increasing numbers of precision supply voltages, leads to considerable difficulties in selecting suitable low cost circuits for a given purpose that can provide high energy-conversion efficiency and which have a relatively simple construction.

A typical prior art switching power supply configuration is illustratively shown in FIG. 1. A primary circuit 10 including at least one switch controlled by a pulse-width modulated square wave

signal is connected to a plurality of loads LD_1, LD_2, LD_3 via respective secondary circuits 12. The secondary circuits 12 may be buck converters, for example, which are well known to those skilled in the art.

The main supply output with respect to the load LD_1 is regulated by a feedback path to the primary 10 which includes a PWM control circuit 14 for modulating the pulse width of the switch control signal at a fixed frequency. The control circuit 14 regulates the output voltage V_{o1} by countering variations in the load LD_1 or in the input voltage V_{in}.

A variation in the input voltage is compensated by the effect of the PWM regulation on all of the outputs. In contrast, a variation in the load LD_2, LD_3, which causes alterations in the output voltages V_{o2} and V_{o3} cannot be taken into account by the PWM control circuit 14, since the two outputs are in an open-loop configuration.

To regulate the output voltages V_{o2} and V_{o3} when there are variations in the load, a regulator circuit 16 is arranged in cascade for each output voltage. Prior art approaches for constructing regulator circuits in cascade include linear regulators, cascaded DC/DC converters, and magnetic amplifiers.

A linear regulator is relatively simple, inexpensive, and easy to design. One significant disadvantage thereof is its low efficiency. For this reason, linear regulators are primarily used exclusively in low current applications.

DC/DC converters arranged in cascade with the output have performance advantages in terms of efficiency, voltage regulation, and permissible current. However, they are disadvantageous from a cost standpoint since a DC/DC converter requires the use of power switches, inductors, capacitors, and control

circuits. Moreover, the introduction of such a converter gives rise to additional noise and produces a ripple in the output current. This ripple has to be corrected by filters, or by synchronizing the regulator with the main PWM control circuit.

Magnetic amplifiers can be described as regulators in cascade with programmable delay switches and are the most common choice for medium and high-power cascade regulators. The main component of such regulators is a reactive component which can be saturated to act as a magnetic switch, since it has high impedance when non-conductive and low impedance when saturated.

The magnetic amplifier achieves a desired control and regulation function and is a relatively simple circuit. It also provides safe performance with large loads. Yet, with a low load or no load, on the other hand, regulation is less efficient. Further disadvantages are that it provides limited switching frequency and may be rather large or bulky to implement.

An effective approach within a wide power range for multi-output switching power supplies and, in particular, in medium or high-power applications, is the cascaded PWM regulator. This regulator includes an auxiliary switching device (generally, but not exclusively, a MOSFET power transistor) controlled by a PWM signal. The PWM signal is generated by a control circuit synchronized with the main PWM control circuit 14.

The regulator preferably works by time modulation of the leading edge of the PWM control signal over time. The auxiliary switch blocks propagation of the voltage signal established in the secondary winding to the output of the power supply. The control circuit of the cascade regulator

synchronizes the conduction periods of the main circuit switch and the auxiliary switch with the trailing edges of the respective square-wave control signals.

The advantages of this regulator over magnetic amplifier regulators are lower cost, smaller dimensions, greater reliability, and better performance. The circuits required to control the switch may be complex, but they may be integrated in a single chip which helps to offset this complexity.

The operation of a control circuit for a cascaded PWM regulator is similar to that of a voltage converter/reducer (i.e., a buck converter). That is, it controls a switch device that is suitable for blocking an input voltage for a predetermined period of time, producing at the output a duty cycle less than that present at the input. The voltage value at the output consequently depends on the feedback loop of the control circuit, which controls the conduction or non-conduction of the switch.

Examples of PWM regulator circuits connected in cascade are described, for example, in U.S. Patent Nos. 6,130,828 and 6,222,747. The '828 patent, which is assigned to Lucent Technologies, relates to a multi-output converter with self-synchronized pulse-width modulated regulation. The PWM control signal of the auxiliary switch associated with the regulator is generated by direct control of a driver circuit with input hysteresis by a ramp signal. This signal is generated by an integrator circuit disposed downstream from a circuit for amplifying the voltage error present at the regulated output. The amplitude of the signal thus depends on the output voltage error to be compensated by the regulator.

The '747 patent, which is assigned to Artesyn Technologies, relates to a control circuit connected in cascade in a multi-output switching power supply. The

circuit described therein includes a synchronous pulse generator arranged to detect the trailing edge of the voltage established in the secondary transformer winding. A ramp signal generator is controlled by the pulses emitted from the pulse generator. The ramp signal generator is connected to the non-inverting input of a comparator, the inverting input of which receives a signal that is indicative of the output-voltage error. This signal is emitted by an error amplifier circuit that can compare the voltage at the output of the regulator with a predetermined internal reference voltage.

The ramp signal is reset and triggered at the same moment in time, which coincides with the trailing edge of the voltage in the secondary transformer winding. A theoretical duty cycle to be achieved in controlling the auxiliary switching device is 100%. That is, an operative condition in which the switching device is always conducting is envisaged.

Summary of Invention

An object of the present invention is to provide a PWM regulator which has a relatively simple and inexpensive circuit construction.

According to the present invention, this object is achieved by a control circuit for a PWM regulator circuit having the characteristics specified in Claim 1.

Brief Description of the Drawings

Further characteristics and advantages of the invention will be explained in greater detail in the following detailed description of an embodiment thereof, which is provided by way of non-limiting example with reference to the appended drawings, in which:

FIG. 1 (previously described) is a schematic circuit diagram of a regulated, multi-output power supply of the prior art;

FIG. 2 is a schematic circuit diagram of a portion of the power supply of FIG. 1, provided with a cascade pulse-width modulated regulator and control circuit in accordance with the present invention;

FIGS. 3 and 4 are timing diagrams showing two series of waveforms that are indicative of the behavior over time of certain electrical quantities of the regulator circuit of FIG. 2, in two different modes of operation;

FIG. 5 is a schematic circuit diagram illustrating the control circuit of FIG. 2 in greater detail; and

FIG. 6 is a timing diagram showing a series of waveforms illustrating certain electrical quantities of the control circuit shown in FIG. 5.

Detailed Description of the Preferred Embodiments

With reference to FIG. 2, a PWM cascaded regulator for multi-output power supplies in accordance with the present invention is now described. The voltage signal V_{s1} is established in the secondary winding of the power-supply transformer. The regulator includes an auxiliary switching device SW, and the voltage signal V_{s2} is downstream of the switch.

When the switch SW is made non-conductive, it blocks the propagation towards the output filter LC of the voltage signal V_{s1} present in the secondary transformer winding. When the switch SW is made conductive, the voltage V_{s1} is established almost unchanged at the terminals of the diode D.

The voltage signal V_d at the terminals of the diode D is thus a pulse width modulated waveform suitable for producing a direct current output via the

filter LC. The pulse width of V_d is controlled by the duty cycle of the main switch M1 of the primary winding and by the operation of the auxiliary switch SW. The main output V_{O1} is regulated by the PWM control circuit 14, and the output V_{O2} is regulated by the operation of a feedback control circuit 20.

Turning now to FIG. 3, the waveforms of the signals V_{s1}, V_{s2}, V_d of the PWM regulator (from which the state of the associated switch SW can be inferred), and of the current passing through the inductor L in a continuous-conduction mode of operation are illustratively shown. The conduction and non-conduction intervals of the primary switch M1 are indicated as t_{on1} and t_{off}, respectively, and T_s is the switching period.

The interval during which the auxiliary switch SW is non-conductive is indicated as t_b. The time interval during which the auxiliary switch SW is conductive and the transfer of power takes place between the input and output is indicated as t_{on2}. The positive voltage V_d brings about an increase in the inductor current I_L, whereas an absence of voltage brings about the discharge of the inductor. The auxiliary switch SW is thus non-conductive during the interval $t_{off} + t_b$.

The mode of operation with discontinuous inductor conduction, to which the foregoing discussion also applies, is shown in FIG. 4. If the parasitic elements are ignored, a positive voltage equal to V_{O2} appears as the voltage V_d in the time interval t_d, during which the inductor current is zero.

With reference to FIG. 5, the control circuit 20 according to the invention comprises a detector circuit 22 for detecting the trailing edge of the square wave voltage signal V_{s1}, which is present at the terminals of the secondary transformer winding. A ramp-signal generator circuit 24 is connected to the output

of the detector circuit 22 and is connected, by way of its own output, to the non-inverting input of a comparator 26. The inverting input thereof receives a signal from an error amplifier circuit 28 connected to the output of the power supply.

The error amplifier circuit 28 includes an operational amplifier OA in a non-inverting configuration. The output voltage V_{02} of the power supply is fed back from the output to the non-inverting input terminal and is compared with a predetermined reference voltage V_{REF} applied to the inverting input terminal. It should be noted that this is in contrast to what is described in the above-noted references.

The output of the comparator 26 is connected to a set input S of a bistable circuit 30, such as an S-R flip-flop. The reset input R thereof receives the signal emitted by the detector circuit 22 after it has passed through a delay block 32 (e.g., a conventional delay line). The operation of the bistable circuit 30 is regulated in accordance with the following truth table:

S	R	Q
0	0	Q_{prec}
1	0	1
0	1	0
1	1	1

The direct output Q of the flip-flop 30 is connected to a high-side driver circuit 34 for driving the switch SW, which may be formed as a bipolar transistor or, preferably, as a power MOSFET.

Referring now to the timing diagram of FIG. 6, the square wave voltage signal V_{s1} at the terminals of the secondary transformer winding is supplied as an input to the detector circuit 22. This circuit

generates a pulse coinciding with each trailing edge of the waveform of the voltage V_{s1}. This pulsed signal is indicated as RESET in the drawings and is supplied as an input to the ramp generator circuit 24 and to the delay block 32.

The ramp generator circuit 24 triggers the generation of a ramp signal V_{ramp} with each leading edge of the signal V_{s1}, and it resets its own output when it receives the RESET pulses which are synchronous with the trailing edges of V_{s1}. The overall signal V_{ramp} over time has a sawtooth-like waveform, as illustratively shown. The signal V_{err} emitted by the error amplifier circuit 28 is applied to the inverting input of the comparator 26 and compared with the signal V_{ramp} emitted by the ramp generator circuit 24.

The comparator circuit 26 generates at its own output a square wave signal V_{comp} (not shown) which is positive when V_{ramp} is greater than V_{err}, and which has a duty cycle less than that of the voltage signal v_{s1}. The signal V_{comp} is applied to the set input S of the bistable circuit 30 to establish, at its output, a control signal V_{PWM} for the driver circuit 34 of the switch SW.

The S-R bistable circuit 30 causes operation to be at a constant frequency if the waveforms V_{ramp} and V_{err} do not intersect at any point. The delay block 32 is interposed in the path of the RESET signal before the reset input R of the bistable 30 so that the switching of the reset signal to a low logic level takes place only after the signal V_{comp} emitted by the comparator circuit 26 to the set input S of the bistable circuit has also reached a low logic level.

The signal V_{PWM} for driving the switch SW therefore also has a duty cycle less than that of the signal V_{s1}, with modulation of the leading edge over time and with the trailing edges coinciding. When the

voltage value of the signal V_{err} relating to the error in the power supply output voltage is less than the voltage value of the signal V_{ramp}, the duty cycle of the driving signal V_{PWM} is equal to the duty cycle of the signal V_{s1}.

Advantageously, resetting of the ramp signal coincides with the trailing edge of the voltage signal in the secondary transformer winding. Yet, its triggering coincides with the leading edge of the voltage signal in the secondary winding. This is in contrast to the circuit described in U.S. Patent No. 6,222,747, in which its resetting and triggering take place at the same moment, coinciding with the trailing edge.

The maximum duty cycle that can be reached in the control of the auxiliary switch is equal to the duty cycle of the primary circuit. The amplitude of the ramp signal generated is fixed and depends on the configuration of the generator circuit 24 used, and not on the error in the voltage output by the power supply as described in U.S. Patent No. 6,130,828.

With respect to the circuit described in the '828 patent, the ramp signal for controlling the auxiliary switch is reset by superimposing the signal V_{s1} of the voltage in the secondary transformer winding. By contrast, the control circuit 20 of the present invention makes use of the circuit 22 for detecting the trailing edges of the voltage V_{s1} to control the resetting of the ramp signal with instantaneous precision.

Moreover, in the circuit according to the present invention, the ramp signal is synchronized with the voltage signal V_{s1} by the trailing edge detector circuit 22. Yet, in the circuit described in the '828 patent, this takes place by way of a freewheeling diode

connecting the integrator circuit to the high voltage terminal of the secondary transformer winding.

The control circuit according to the invention advantageously enables common-cathode diodes, which are in widespread use and are readily obtainable at low cost, to be used for the construction of the voltage converter/reducer configuration in the secondary winding of the power supply. The power inductor of the voltage converter/reducer can be arranged either in the positive voltage branch or in the ground branch. This is in contrast with many prior art regulators for switching power supplies that allow for arrangement solely in the ground branch, such as, for example, the Unitrode devices produced by Texas Instruments and sold under the part numbers UCC1583/4, UCC2583/4, UCC3583/4.

The exemplary configuration described above may also be used in a power supply with a transformer having only one secondary winding for serving two outputs. One of the outputs is controlled by the primary PWM control circuit, and the other is controlled by a PWM regulator in cascade.

Since the control circuit according to the present invention has an error amplifier circuit having the reference voltage applied to its own inverting input, unlike the circuits of the prior art, it does not need an output inverter device. Consequently, it may be produced with the use of a smaller number of components.

Of course, the principle of the invention remaining the same, the forms of embodiments and details of construction may be varied widely with respect to those described and illustrated herein purely by way of non-limiting example, without departing from the scope defined in the following claims.